A −12.3 dBm UHF Passive RFID Sense Tag for Grid Thermal Monitoring

Bo Wang, *Member, IEEE*, Man-Kay Law, *Senior Member, IEEE*, Jun Yi, *Member, IEEE*, Chi-Ying Tsui, *Senior Member, IEEE*, and Amine Bermak, *Fellow, IEEE*

***Abstract*—This paper presents an ultra-high-frequency (UHF) passive sense tag for electrical grid and substation thermal monitoring, with emphasis on the tag system optimization and the design of a low power embedded temperature sensor. The designed tag achieves a sensitivity of −12.3 dBm under active temperature monitoring operation, which is the state of the art among existing UHF passive temperature sense tag products. The sensing inaccuracy of the tag is ±2.5 °C (3σ) from −25 to 120 °C after a low-cost wireless single-point trim. An antimetal ceramic-packaged tag was tested by attaching to a ring main unit in the substation and complete tag system demonstrated robust wireless operation with a sensing distance of 3.5 m. The combination of batteryless and wireless operation, high sensitivity, wide sensing range, and small incident-power-dependent error (±0.2 °C) makes this tag suitable for the target applications.**

***Index Terms*—Antimetal antenna, CMOS temperature sensor, grid thermal monitoring, radio-frequency identification tag (RFID) temperature sense tag, relaxation clock generator, ultra-high-frequency (UHF) RFID.**

I. Introduction

In electrical grid and substation applications, equipment like switchgear, ring main unit, etc., are often the last line of defense for protecting the end users [1]. Failures of the equipment could cause long outages, huge economic losses, and present threats to public safety. As reported in [2], the major causes of grid equipment failures are loose or corroded metal connections, degraded cable insulation, and external agents (e.g., dust and water). Due to ohmic loss at these weak points, potential failures are always accompanied with increased thermal signatures over time, which can be predicted via continuous thermal monitoring solutions [3].

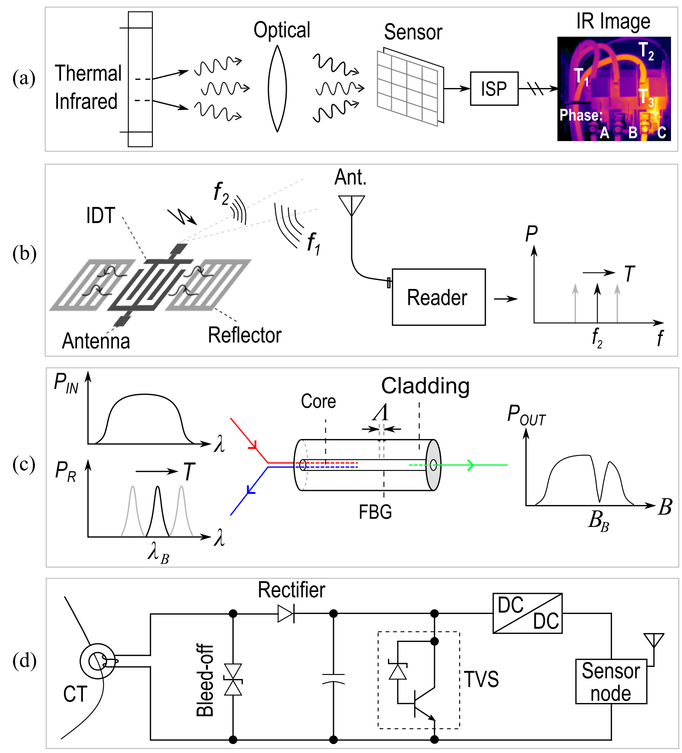


Fig. 1. Illustration of (a) infrared; (b) SAW; (c) FBG; and (d) CT-powered systems for grid thermal monitoring.

As shown in Fig. 1, several existing systems have been proposed for grid thermal monitoring, including infrared radiation (IR) imaging, surface-acoustic-wave (SAW) sensing, fiber-Bragg-grating (FBG) system, and wireless sensor powered by current transformers (CT) [1], [4]–[7]. However, these solutions are still not widely deployed due to their respective drawbacks. For example, the line-of-sight requirement between the sensor and the target object makes it impossible for IR imaging to access all critical thermal spots. As the signal from SAW sensor is weak and in analog form, the strong electromagnetic (EM) noise environment surrounding the substation would jeopardize its operation [3]. Apart from that, as SAW devices are not individually addressable, only a few sensors can be deployed in a confined space [1]. Even though FBG sensing systems are resistant to EM noise, they are sensitive to mechanical strain, which

Manuscript received July 21, 2018; revised October 11, 2018 and November 16, 2018; accepted December 16, 2018. Date of publication January 14, 2019; date of current version June 28, 2019. *(Corresponding author: Bo Wang.)*

B. Wang and A. Bermak are with the Division of Information and Computing Technology, College of Science and Engineering, Hamad Bin Khalifa University, Doha 34110, Qatar (e-mail: bwang@hbku.edu.qa; abermak@hbku.edu.qa).

M. K. Law is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China (e-mail: mklaw@umac.mo).

J. Yi is with Zhejiang Yuehe Technology, Hangzhou 310000, China (e-mail: yijun@johar.cn).

C. Y. Tsui is with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong (e-mail: eetsui@ust.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2019.2891447

inevitably leads to high packaging cost to alleviate the strain produced during installations [5]. The fragility of the fiber also makes it an inferior choice [6]. Despite the wireless sensing capability of CT-powered systems through harvesting energy from the grid with small transformers [7], the requirement of grid renovation for CT installations, together with repetitive testing with the active grid, ultimately makes this solution impractical.

Considering the large amount of thermal spots inside the electrical grid and substation, the sensing device should be low-cost and easily retrofitted to the equipment (e.g., with bolted connection) [8]. Meanwhile, to avoid adverse effects such as arcing, the device that has direct contact with energized conductors should be cable- and battery-free [3]. Passive ultra-high-frequency (UHF) radio-frequency identification tag (RFID) is capable of meeting all these requirements. However, embedding a temperature sensor inside the tag while achieving the performance required for the target application is a nontrivial task [9]. First, the sense tag must cover the normal busbar operation temperature range of $-5 \sim 110$ °C [10], [11]. In addition, in substations (< 360 kV), the maximum restricted approach distance to energized conductors is 2.8 m [12]. Therefore, the sense tag's minimum reading distance should be greater than 3 m to allow safe operation in practical scenarios. This corresponds to a tag IC sensitivity of about -5 dBm (calculated with a 35% rectifier efficiency, zero path loss, 4 W effective isotropic radiated reading power (EIRP), and 0 dBi tag antenna gain [13]). Consequently, the limited sensing range ($-40\sim85$ °C in [15] and $-40\sim60$ °C in [16]) and/or tag sensitivity ($+0.85$ dBm in [17] and -2 dBm in [18]) in existing passive sense tag products still fall short of meeting the target grid thermal monitoring requirements[15]–[19].

This paper presents a passive sense tag designed for electrical grid thermal monitoring, with contributions including (a) tag system optimization for high sensitivity; (b) a time-domain embedded sensor for wide range and low power sensing; and (c) a sensor data retrieving scheme to avoid power-hungry multi-time programmable (MTP) memory writings. The designed tag achieves a -12.3 dBm sensing sensitivity and exhibits only ±0.2 °C incident-power-dependent sensing error. The ceramic packaged tag also shows a nominal sensing distance of 3.5 m when tested on a ring main unit in the substation. The remainder of this paper is organized as follows. Section II presents the tag optimization and sensor design. The measured sense tag performance and package for grid application are introduced in Section III. Section IV concludes this paper.

II. Tag Optimization and Sensor Design

The designed passive tag system is shown in Fig. 2. It consists of an RF energy harvester, a baseband clock generator, a temperature sensor, a modulator/demodulator, an MTP memory, and a data storage cell. During operation, the capacitor C_{R} (several nF) at the rectifier output stores the harvested RF energy. If the voltage V_{CR} of this capacitor satisfies $V_{\mathrm{CR}} \geq V_{\mathrm{min}}$ (minimum operation voltage of the tag, e.g., 1.6 V) within the 2.5 ms startup time (EPC protocol [20]), the tag can be activated. To sustain the operation of this tag, its harvested RF energy should balance

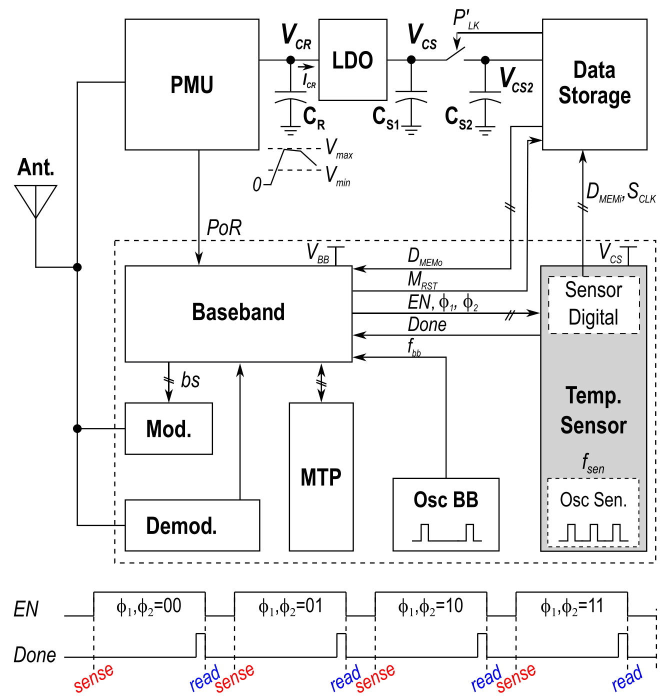


Fig. 2. Simplified block diagram of the sense tag (regulator to generate the baseband supply $V_{\mathrm{BB}} = 0.8$ V is not shown); and the interface timing diagram between the sensor and the baseband.

its energy consumption $\int V_{\mathrm{CR}}(t) \cdot I_{\mathrm{CR}}(t)dt$ in any short time intervals (e.g., a few μs, I_{CR}(t) is the current flowing out of C_{R}) to avoid large V_{CR} drop. Therefore, different from active-/battery-assisted-passive (BAP) tags and tags with other energy sources [21], [22], the sensitivity of RF-powered tag, P_{tag} (commonly expressed in dBm), is limited by its power consumption instead of its communication link loss, and can be estimated by

$$P_{\mathrm{tag}} = \frac{1}{t_1 - t_2}\frac{1}{\overline{\eta}_{\mathrm{rec}}}\int_{t_1}^{t_2} V_{\mathrm{CR}}(t)I_{\mathrm{CR}}(t)dt \tag{1}$$

where $\overline{\eta}_{\mathrm{rec}}$ is the average rectifier efficiency within a time interval $t_1\sim t_2$. According to (1), the power and spike current of all sensing circuits should be minimized in order to optimize P_{tag}. However, previous efforts on sense tags mainly focused on the designing of low-power sensors [9], [23]. This paper targets on systematic considerations of the sensing block within the tag system to achieve system level co-optimization (e.g., peripheral circuits, control, data processing, and storage).

A. System Power Optimization

Fig. 3 shows the typical reader commands and tag replies in a complete sensing cycle following the EPC protocol [20]. The reader commands include tag select (*select*), tag inventory (*Query*, *Ack*, *QueryRep/Nak*), and tag access (*Sense*, *MTP read*). The corresponding tag replies include the random number RN16, the EPC, and the sensor data. To minimize P_{tag}, our tag system is first optimized by identifying and powering down noncritical circuit blocks in different command phases. For example, the modulator, demodulator, and most of the baseband are disabled during sensing. The optimized power distributed

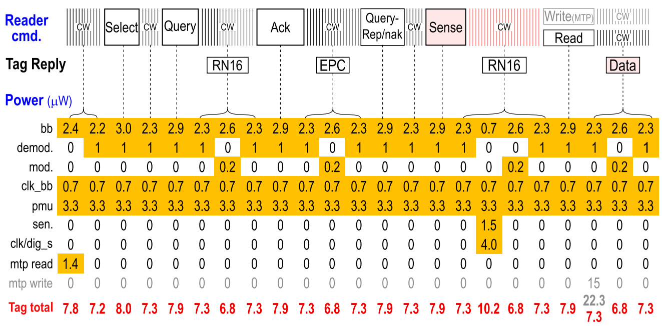


Fig. 3. Optimized tag power profile in different command phases (MTP write power is shown in gray and is eliminated in this paper). The power consumption data of most blocks are from [9], [23].

to different circuit blocks (baseband, demodulator, modulator, baseband clock, power management unit, sensor, sensor clock, sensor digital, and MTP) in different time intervals are also included in Fig. 3. Particularly, though the tag baseband is always active, its power is dynamically optimized according to the received command. After optimization, a large sensor power of 5.5 μW will only degrade the tag sensitivity by 1 dBm compared with its inventory phase. However, if the sensor data have to be stored in the MTP before being read out as in [15] and [16], the large MTP writing power would significantly degrade the tag sensitivity. For example, a writing power of 15 μW [24] will reduce the tag sensitivity by 4.5 dBm based on the data in Fig. 3. Fortunately, as mature communication infrastructures are available in the grid/substation, the sensor data can be transmitted to the base station for storage. In this paper, a custom data storage cell is designed (see Section II-C) so that the sensor data can be retrieved directly by the reader after sensing to ensure the data integrity while avoiding power-hungry MTP writings.

For normal sensing operation, $V_{\mathrm{CR}} \geq V_{\min}$ of the tag should always hold. However, the output power P_{out} of a reader is not always constant due to its frequency hopping property [25]. The fluctuation of P_{out} may cause instantaneous V_{CR} drop and increase the error rate of the sensor output. To address this issue, V_{CR} in this tag is charged to a higher voltage $V_{\max} = 2$ V (limited by the process) before sensing. Therefore, the excess energy $C_{\mathrm{R}}(V_{\max} - V_{\min})$ can temporarily balance the energy consumed by the tag to achieve robust sensing even when the incoming RF energy is insufficient or absent. For example, when $P_{\mathrm{out}} = 0$, a C_{R} of 100 nF can solely sustain a tag for 4 ms (assuming a 10 μA load and a voltage drop of 400 mV on C_{R}). In this design, C_{R} is sized to be 1.85 nF to maintain a reasonable chip size. It allows an RF-off time of about 100 μs during sensing, which is comparable to the reader's switching time (e.g., blanking interval) due to frequency hopping.

B. Embedded Sensor Design

1) Sensing Principle: Besides system optimization, a power-efficient sensor is also essential to minimize P_{tag}. As shown in Fig. 2, under normal conditions, the sensor is mainly supplied by a 1.45 V regulated output V_{CS} (sensor digital is supplied by the 0.8 V V_{BB} for low power). When the reader issues a sensing command, an EN signal from the baseband will activate the sensor and the sensor clock generator (see Section II-B4). Meanwhile, most functions of the baseband are disabled for power savings. At the end of the sensing conversion, the sensor generates a $Done$ signal to bring the baseband back to its normal operation to reply the reader's sensing request.

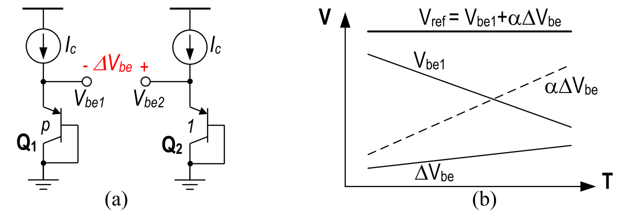


Fig. 4. (a) Diode-connected PNPs with a collector biasing current density ratio of p. (b) Ratio of a PTAT voltage $\alpha\Delta V_{\mathrm{be}}$ and reference voltage V_{ref} is a measure of temperature [28].

As reported, MOSFET-based sensors can achieve ultra-low power operation (e.g., 0.1 μW in [26] and [27]). However, because of the carrier mobility and threshold voltage variation of MOSFET, a two-point trim is required to achieve a $\pm 1\%$ precision, which inevitably increases the tag cost [28]. To trim the tag at a single temperature and achieve a wide sensing range, this design uses the vertical substrate parasitic PNP bipolar junction transistor (BJT) as the sensing device. This BJT is available in the adopted standard CMOS process and does not require extra masks for fabrication [28]. As in Fig. 4(a), for two diode-connected BJTs $Q_{1,2}$, their base-emitter voltages

$$V_{\mathrm{be}1,2} = V_{\mathrm{T}} \cdot ln \frac{I_{\mathrm{c}}}{I_{\mathrm{s}1,2}} \tag{2}$$

are complementary-to-absolute-temperature (CTAT), where V_{T} is the thermal voltage (26 mV at 300 K), I_{c} is their collector bias current, $I_{\mathrm{s}1,2}$ are their saturation currents, respectively [28]. If the emitter area ratio of $Q_{1,2}$ is p, $I_{\mathrm{s}1} = p \cdot I_{\mathrm{s}2}$ holds. Therefore, the emitter-base voltage difference of $Q_{1,2}$ is

$$\Delta V_{\mathrm{be}} = V_{\mathrm{be}2} - V_{\mathrm{be}1} = V_{\mathrm{T}} \cdot ln(p) \tag{3}$$

which is proportional-to-absolute-temperature (PTAT). As shown in Fig. 4(b), one can digitize $\alpha\Delta V_{\mathrm{be}}$ against another voltage $V_{\mathrm{ref}} = V_{\mathrm{be}1} + \alpha\Delta V_{\mathrm{be}}$ to obtain the digital representation of the tag temperature [29], where α is a proportional constant to make V_{ref} temperature-independent.

2) Temperature Sensor Front-End: The designed sensor front-end is shown in Fig. 5. $Q_{1,2}$ with an emitter area ratio of $p = 4$ are the BJT sensing devices and they have the same collector bias current (from the current mirror $M_{\mathrm{p3,p5}}$, $M_{\mathrm{p4,p6}}$). The switches $S_{1\text{–}4}$ controlled by ϕ_1 and ϕ_1' can swap the currents flow into $Q_{1,2}$. During operation, $Q_{1,2}$, a resistor R_{pt}, an amplifier A_1 (current mirror loaded differential pair), MOSFETs $M_{\mathrm{n1,n3}}$ and $M_{\mathrm{p3\text{-}p8}}$ form a negative feedback loop (stabilized by R_z and C_{c}). This loop ensures $V_{\mathrm{x}} = V_{\mathrm{be}2}$. Therefore, the voltage across R_{pt} is V_{x}–$V_{\mathrm{be}1} = \Delta V_{\mathrm{be}}$ and a PTAT current I_{pt} (nominal 77 nA) is generated via R_{pt}. To minimize the finite loop-gain

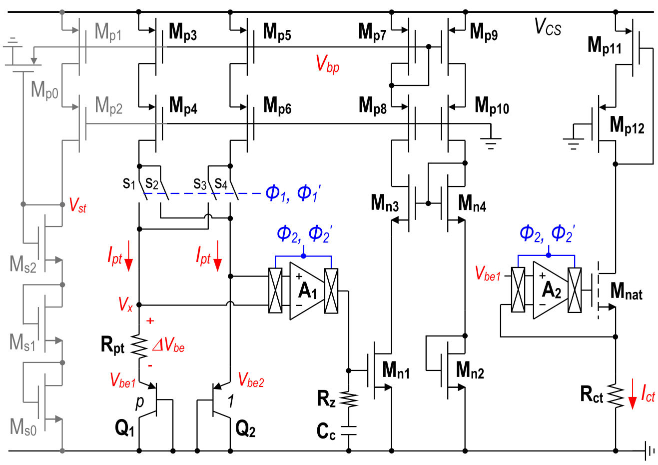


Fig. 5. Sensor front-end to generate I_{pt} and I_{ct} (start-up circuit in gray).

induced error in I_{pt}, the positive feedback formed by $M_{\mathrm{p7–p10}}$ and $M_{\mathrm{n3,n4}}$ boosts the overall loop gain to $\sim$95 dB. The CTAT current $I_{\mathrm{ct}} = V_{\mathrm{be1}}/R_{\mathrm{ct}}$ (nominal 100 nA) is generated via the V–I converter formed by the amplifier A_2 (folded-cascode topology), a native transistor M_{nat}, and a resistor R_{ct}. In Fig. 5, $M_{\mathrm{p0–p2}}$ and $M_{\mathrm{s0–s2}}$ form a start-up circuit. After power-up, $V_{\mathrm{st}} = 0$ and $V_{\mathrm{bp}} = V_{\mathrm{CS}}$, current in M_{p0}, then gradually discharges V_{bp}, which would finally enable the operation of feedback loop to generate the desired I_{pt}. Once I_{pt} is large enough, V_{st} developed by $M_{\mathrm{s0–s2}}$ turns M_{p0} OFF and the front-end enters into its normal operation mode. The total current consumption of this front-end is 0.9 μA.

Similar to [31], the systematic nonlinearities of $I_{\mathrm{pt,ct}}$ due to the BJT current gain (nominal 2.6) is canceled in the digital back-end using a nonlinear digital to temperature transfer curve (third-order curve fitting). In Fig. 5, mismatches of $M_{\mathrm{p3–p6}}$, $Q_{1–2}$ and offsets in $A_{1,2}$ would also degrade the precision of $I_{\mathrm{pt,ct}}$. Typically, dynamic element matching (DEM) and chopping were used to suppress these errors [31]. In this design, instead of performing DEM, four temperature samples with different ϕ_1, ϕ_2 (from the reader command and decoded by the tag baseband) will be collected, as shown in Fig. 2. In this way, the static device offset errors can be averaged out at the reader side. Moreover, one complete temperature reading is divided into four samples and the charge stored in C_{R} can be refilled before each sampling. As a result, the tag becomes more resistant to random P_{out} drop during frequency hopping [25].

3) Time-Domain Sensor Readout: The designed sensor readout and its timing diagram are shown in Figs. 6 and 7, which is an improved dual-slope A/D. Before each conversion, the integration capacitor C_{pos} is reset by $\mathrm{RST_p}$. Then, the current $I_{\mathrm{pt\_sen}}$–$I_{\mathrm{ct\_sen}}$ controlled by INTE is used to charge up C_{pos}. Once the voltage V_{pos} exceeds a reference voltage V_{ov} ($\sim$250 mV in this design), the output T_{pos} of the continuous-time comparator $\mathrm{A_3}$, will be activated (rising-edge), indicating that V_{pos} is high enough to maintain the operation of the current sink $I_{\mathrm{ct\_sen}}$. After this rising-edge, C_{pos} will be charged for another N clock cycles before being discharged by a reference current $I_{\mathrm{ref\_sen}}$ controlled by $\mathrm{DIS_p}$. During discharge, once $V_{\mathrm{pos}} < V_{\mathrm{ov}}$, T_{pos}

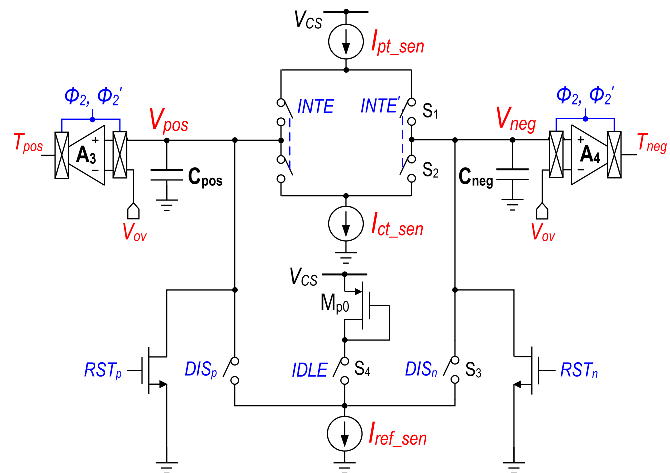


Fig. 6. Dual-slope A/D with ping-pong-like operation. Refer to Fig. 5, $I_{\mathrm{pt\_sen}} = I_{\mathrm{pt}}$ and $I_{\mathrm{ct\_sen}} = 0.4 I_{\mathrm{ct}}$ to utilize the A/D's dynamic range [28]. $C_{\mathrm{pos,\,neg}} = 12.5$ pF.

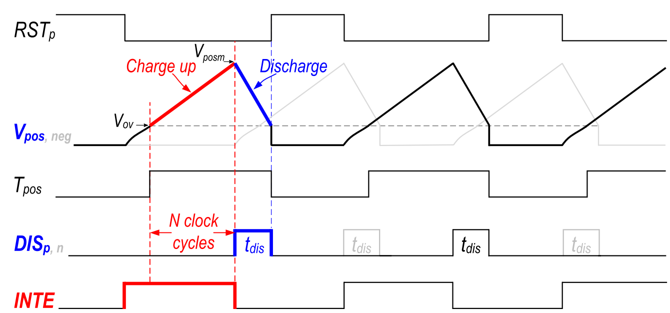


Fig. 7. Sensor readout timing diagram (for simplicity, $\mathrm{RST_n}$, $\mathrm{DIS_n}$, and IDLE are not shown; four t_{dis} are averaged in one sample to minimize clock and substrate noise induced error).

will be deactivated (falling-edge) and C_{pos} is reset again. For charge conservation of C_{pos}

$$V_{\mathrm{posm}} - V_{\mathrm{ov}} = \frac{I_{\mathrm{pt\_sen}} - I_{\mathrm{ct\_sen}}}{C_{\mathrm{pos}}} \frac{N}{f_{\mathrm{sen}}} = \frac{1}{C_{\mathrm{pos}}} I_{\mathrm{ref\_sen}} t_{\mathrm{dis}} \tag{4}$$

where V_{posm} is the voltage on C_{pos} after integration, f_{sen} is the sensor clock frequency, and t_{dis} is the time required to discharge C_{pos} until the falling-edge of T_{pos} is triggered. Therefore

$$t_{\mathrm{dis}} = \frac{N}{f_{\mathrm{sen}}} \frac{I_{\mathrm{pt\_sen}} - I_{\mathrm{ct\_sen}}}{I_{\mathrm{ref\_sen}}}. \tag{5}$$

If t_{dis} is quantized by f_{sen}, the digital sensor output is

$$D_{\mathrm{o}} = t_{\mathrm{dis}} \cdot f_{\mathrm{sen}} = N \cdot \frac{I_{\mathrm{pt\_sen}} - I_{\mathrm{ct\_sen}}}{I_{\mathrm{ref\_sen}}} \tag{6}$$

which is a linear function of temperature. To achieve a sensing resolution of $\sim$0.1 °C from −25 to 120 °C, N is designed to be 1600. $I_{\mathrm{pt\_sen}}$, $I_{\mathrm{ct\_sen}}$, and $I_{\mathrm{ref\_sen}}$ are 77, 39.75, and 83.9 nA, respectively, at 25 °C.

In this readout, another circuit branch consisting of $S_{1–3}$, C_{neg} and A_4 is added. When C_{pos} is being discharged (charged up), $I_{\mathrm{pt\_sen}}$–$I_{\mathrm{ct\_sen}}$ ($I_{\mathrm{ref\_sen}}$) is diverted to charge up (discharge) C_{neg}, and vice versa, which forms a ping-pong like operation. In this way, the conversion speed can be maximally increased

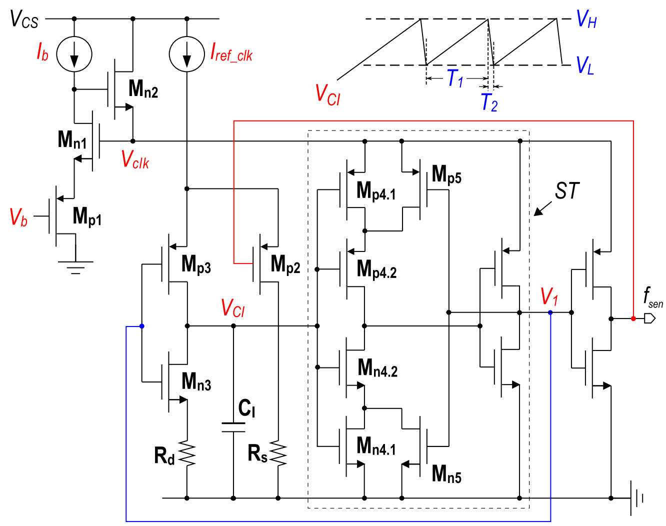


Fig. 8. Proposed process compensated clock generator. $C_{\rm I}$ = 45 fF, $R_{\rm d}$ = 33 kΩ, $I_{\rm ref\_clk}$ = 0.65 μA, $I_{\rm b}$ = 150 nA, $V_{\rm b}$ = 240 mV.

by 2× compared to conventional dual-slope A/Ds [30], [31]. Meanwhile, as $I_{\rm pt\_sen}$, $I_{\rm ct\_sen}$ are always conducting; $I_{\rm ref\_sen}$ is starved by S_4 and $M_{\rm p0}$ during its idle state; there are no large internal voltage swings. Spike current in the readout circuit is thus minimized. Note that the control signals ϕ_2 and ϕ_2' in Fig. 6 is the same as that in Fig. 5 to cancel the comparator offset induced sensing error. The total current consumption of this readout is 0.25 μA.

4) Process-Compensated Clock: To ensure the validity of (4), $V_{\rm posm}$ must be below 1.25 V in order not to drive the current source $I_{\rm pt\_sen}$ into its linear region. At 120 °C, $I_{\rm pt\_sen} = 108.5$ nA and $I_{\rm ct\_sen} = 27.75$ nA, for a nominal $V_{\rm posm}$ of 1.1 V, the required sensor clock frequency $f_{\rm sen}$ is 12 MHz. In the worst case, $f_{\rm sen}$ should be > 10.3 MHz in order to keep $V_{\rm posm} < 1.25$ V. To meet the requirement of $f_{\rm sen}$, a low power process-compensated relaxation clock shown in Fig. 8 is proposed. This clock consists of a pseudo-supply generator, a current source $I_{\rm ref\_clk}$, an integration capacitor $C_{\rm I}$, and a Schmitt trigger (ST). Under the control of the ST, $C_{\rm I}$ is repetitively charged by $I_{\rm ref\_clk}$ for a period of T_1 and discharged by $R_{\rm d}$ for a period of T_2. The ST's effective trip threshold is

$$V_{\rm T} = \frac{V_{\rm clk} - |V_{\rm thp4}| + \sqrt{\eta} V_{\rm thn4}}{1 + \sqrt{\eta}} \tag{7}$$

where $V_{\rm clk}$ is the supply voltage of the ST, $V_{\rm thn4,\,thp4}$ are the threshold voltage of $M_{\rm n4,\,p4}$, respectively, and η is the effective tranconductance parameter ratio of $M_{\rm n4,\,p4}$ [32]. As shown in Fig. 8, the ST involves a positive feedback that controls the effective length of $M_{\rm n4,\,p4}$. When the ST's output V_1 is logic LOW, $M_{\rm p4.1}$ is bypassed by $M_{\rm p5}$ and η is small, the ST's upper trip threshold is $V_{\rm H} \approx V_{\rm clk} - |V_{\rm thp4}|$. When V_1 is logic HIGH, $M_{\rm n4.1}$ is bypassed by $M_{\rm n5}$ and η is large, the ST's lower trip threshold is $V_{\rm L} \approx V_{\rm thn4}$. For a small discharge resistor $R_{\rm d} = 33$ kΩ, $T_1 \gg T_2$ holds. Therefore, the output frequency of the ST is

$$f_{\rm sen} \approx \frac{I_{\rm ref\_clk}}{C_{\rm I}} \frac{1}{V_{\rm H} - V_{\rm L}} = \frac{I_{\rm ref\_clk}}{C_{\rm I}} \frac{1}{V_{\rm clk} - |V_{\rm thp4}| - V_{\rm thn4}}. \tag{8}$$

If $V_{\rm clk}$ is constant, $f_{\rm sen}$ varies significantly due to the spreads and temperature dependencies of $V_{\rm thn4,\,thp4}$. In this paper, a pseudo-supply generator for the ST is proposed to minimize the variation of $f_{\rm sen}$. In Fig. 8, with a reference current $I_{\rm b}$ and voltage $V_{\rm b}$, the pseudo-supply is

$$V_{\rm clk} = |V_{\rm thp1}| + V_{\rm thn1} + \sqrt{\frac{2I_{\rm b}}{K_{\rm p1}}} + \sqrt{\frac{2I_{\rm b}}{K_{\rm n1}}} + V_{\rm b} \tag{9}$$

where $V_{\rm thn1,\,thp1}$ and $K_{\rm n1,\,p1}$ are the threshold voltage and tranconductance parameter of $M_{\rm n1,\,p1}$, respectively. By designing $M_{\rm n1,\,p1}$ and $M_{\rm n4,\,p4}$ with the same size, $V_{\rm thn1,\,thp1} = V_{\rm thn4,\,thp4}$ can hold after dedicated device matching. By replacing $V_{\rm clk}$ in (8) with (9), $f_{\rm sen}$ becomes temperature-, device threshold-, and supply-insensitive (to the first order).

In Fig. 8, a negative feedback consisting of $M_{\rm n1,2}$ is added to stabilize $V_{\rm clk}$ (simulated to be 37 dB dc regulation). Meanwhile, to avoid spike currents during switching, when $C_{\rm I}$ is being discharged, $I_{\rm ref\_clk}$ is starved via $M_{\rm p2}$ and $R_{\rm s}$ with $I_{\rm ref\_clk} R_{\rm s} \approx V_{\rm L}$. After compensation, with a nominal output frequency of $f_{\rm sen}$ = 12 MHz, its variation at different corners is reduced from ±49.7 to ±8.5% for a $V_{\rm CS}$ range of 1.2∼2 V and a temperature range of −25∼120 °C, which meets the target requirement. The total current consumption of this clock generator is 1.35 μA (including bias, bias replica, buffer, etc.).

C. Custom Sensing Command and Data Storage

After embedding this sensor into the tag, custom commands are required to trigger the sensor and read the sensor data, which are nonstandard functions in the EPC protocol [20]. For most EPC G2 commands, the maximum link time (e.g., time interval between the end of the command and the beginning of the tag reply) is only 0.262 ms, which is not long enough for one precision temperature conversion. In [15], the *select* command is utilized to trigger the sensor while it requires 2.5 ms to finish one conversion. Therefore, the sensor enters a “free-running” mode during the command timeout period, which degrades the credibility of the received data as no sensor status information (e.g., insufficient supply, conversion timeout, etc.) can be backscattered. In this paper, a custom scheme using *write 0x0F* to mimic a sensor trigger command is employed, whose timeout duration is 20 ms [20]. For a conversion time of 3.5 ms of our sensor, all tag status during sensing can be collected to identify malfunctions.

After conversion, the sensor data in [15] and [16] are written into the MTPs, which limits their effective sensing sensitivity to be −9.9 and −4.5 dBm, respectively. As explained in Section II-A, our sensor data will be stored in digital registers instead of MTP before being read out. However, due to the RF field discontinuity between the *write* and *read* commands, $V_{\rm CR}$ (see Fig. 2) will drop and the sensor data may lose if not being read within a few milliseconds. To resolve this problem, a custom data storage cell is designed to maximize the data retention time. As shown in Fig. 9, after the digital data $D_{\rm MEMi}$ is shifted into the registers, extra circuits that load $C_{\rm s2}$ (see Fig. 2) will be cutoff by the signal $P_{\rm LK}$ (logic $HIGH$, the first bit of $D_{\rm MEMi}$) or $P_{\rm LK}'$. To ensure the validation of the last data bit $D_{\rm o}\langle 11\rangle$, $P_{\rm LK}$

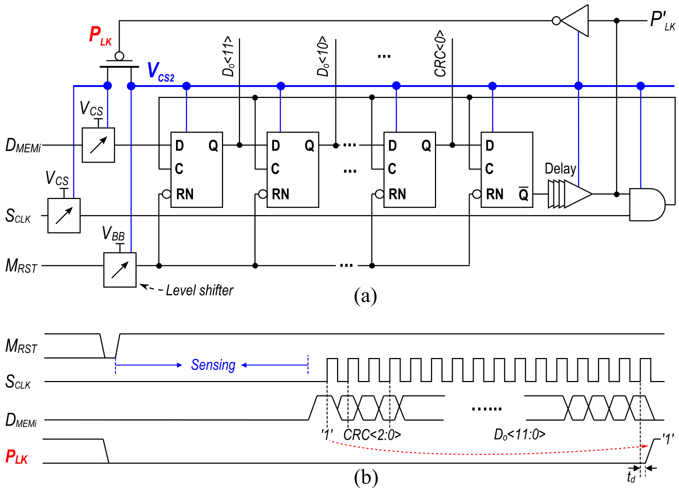


Fig. 9. (a) Data storage cell and (b) its operation timing diagram (P_{LK} is an internal signal of the storage cell).

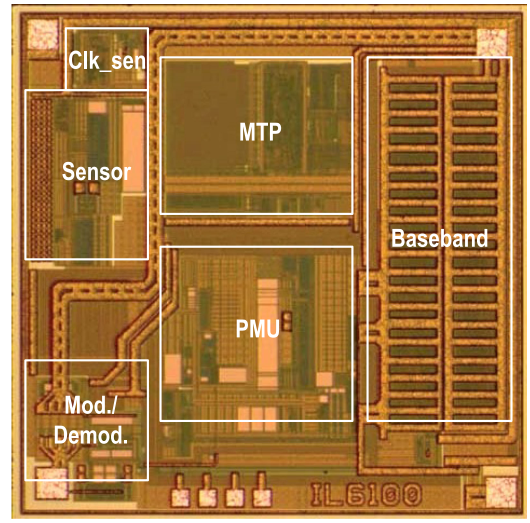
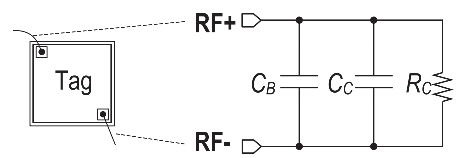


Fig. 10. Fabricated tag micrograph (1.2 × 1.2 mm size).



Para.	Value
C_B	0.20 pF
C_C	0.85 pF
R_C	1.03 kΩ

Fig. 11. Measured tag impedance parameters after chip bumping.

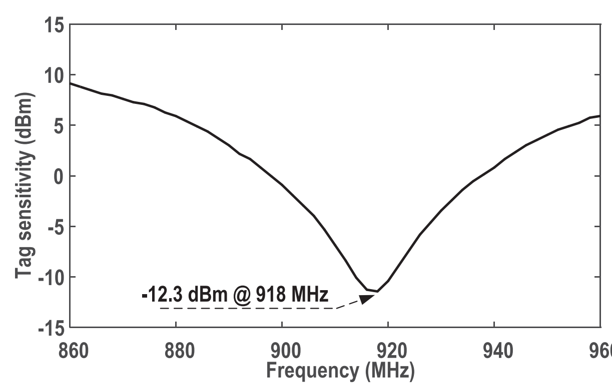


Fig. 12. Tag sensitivity (with sensor enabled) at different frequencies after impedance matched at 920 MHz.

is delayed by t_{d} (21 ns) compared to the last cycle of the shifting clock S_{CLK} [see Fig. 9(b)]. Moreover, a cyclic redundancy check data CRC⟨2:0⟩ is added in D_{MEMi} for data verification when it is read by the reader. In a new sensing cycle, this storage cell will be reset by M_{RST} from the baseband. After optimization, the maximum leakage current loading C_{s2} is 93 pA at 120 °C in the worst case. Since the minimum voltage of C_{s2} is 1.45 V after sensing, the storage cell is designed to operate at a 0.8 V supply. Consequently, a C_{s2} of 200 pF can retain the sensor data for 1.4 s, which is long enough when compared to the ms-level delays of the reader commands. With this scheme, the designed custom *read 0x0F* command can acquire the sensor data D_{MEMo} (see Fig. 2) from this cell instead of the MTP.

III. Experimental Results and Field Application

A. Tag Measurement

The sense tag IC was fabricated in an 8-in engineering wafer in a standard 0.18 μm 1P6M CMOS process. Fig. 10 shows the chip micrograph. The tag input impedance model is shown in Fig. 11, where C_{B} is the bump parasitic capacitance, C_{C} and R_{C} are the measured equivalent tag input capacitance and resistance, respectively. After a conjugate matching of the IC with the antenna at 920 MHz, it is tested with a Voyantic equipment in the EPC Gen2 band (860 to 960 MHz) of the spectrum. As shown in Fig. 12, the achieved tag sensitivity is −12.3 dBm (with a 1.5 dBi antenna gain) at 25 °C to obtain a sensor reading, which corresponds to a chip sensitivity of −10.8 dBm.

To characterize the sensing performance, 54 tags together with a Pt-100 platinum resistor (calibrated to ±0.08 °C precision) were measured in a thermal chamber. The precision of the sense tag is ±2.5 °C (3σ) from −25 to 120 °C after a PTAT trim at 20 °C. In contrast to general purpose sensors, the designed sense tag is calibrated wirelessly by using a reader to read and calibrate multiple tags at the same time. This is more cost-effective than that of [15] with 2-point calibration or [16] that calibrates the sensor at 5 °C. The trim coefficients are stored in the user bank of the MTP before deployment. After trimming, 260 sense tags are measured at 65.3 °C for verification and all the tags' errors (see Fig. 14) are within the 3σ bounds as observed in Fig. 13.

The tag's dynamic performance is tested with a ∼15 °C thermal ramp. Fig. 15(a) shows the fast-tracking property of the tag to the environment temperature changes. The response discrepancy of the sense tag and the Pt-100 during the transition is mainly due to their different thermal time constants. The sensor noise was characterized by 1000 readings at 25 °C. As shown in Fig. 15(b), the thermal noise limited sensing resolution is about 0.17 °C (rms) without averaging, which is enough for the target applications [3].

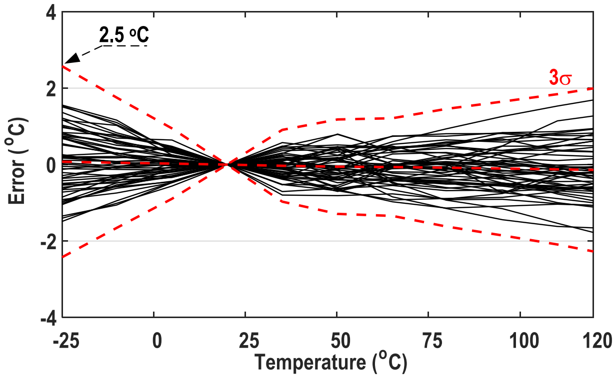


Fig. 13. Measured temperature error of 54 tags after a single-trim at 20 °C and nonlinear correction with a third-order transfer curve; dashed lines refer to the average and $\pm 3\sigma$ limits.

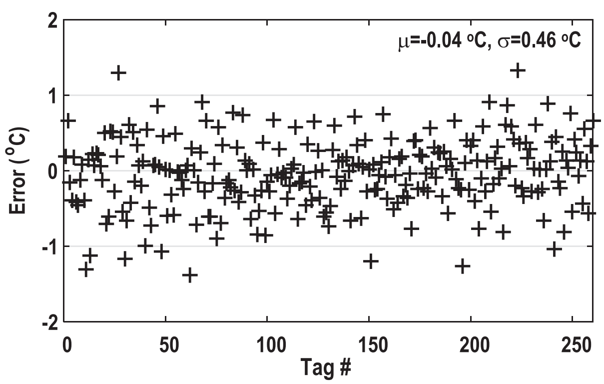


Fig. 14. After single-trim, 260 tags are measured wirelessly at 65.3 °C for verification, showing all the tags are within the error bound in Fig. 13.

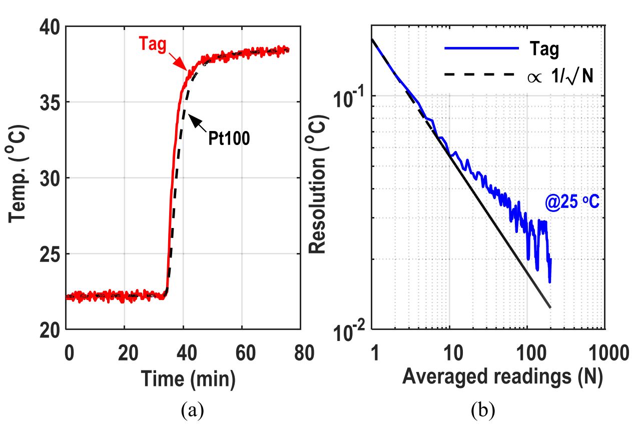


Fig. 15. (a) Step response of the tag; (b) sensing resolution (standard deviation) of the tag versus the number of averaged samples.

For this design, the precharge scheme to mitigate the influences of RF fluctuation and the design of a process-compensated sensor can ensure the robust operation of the tag at different incident power levels. As shown in Fig. 16, only ±0.2 °C error is introduced over a wide 15 dBm incident power range at 30 °C. At higher temperatures, the increased tag power consumption reduces the allowed incident power range, while the power-dependent sensing error is still well-within ±0.2 °C during normal operation. As a result, our proposed solution requires minimal efforts to calibrate the sense tag during field application. Note that all the wireless measurements performed are sampled intermittently (>10 s interval) to avoid the effect of tag self-heating after a prolonged exposure to strong RF field.

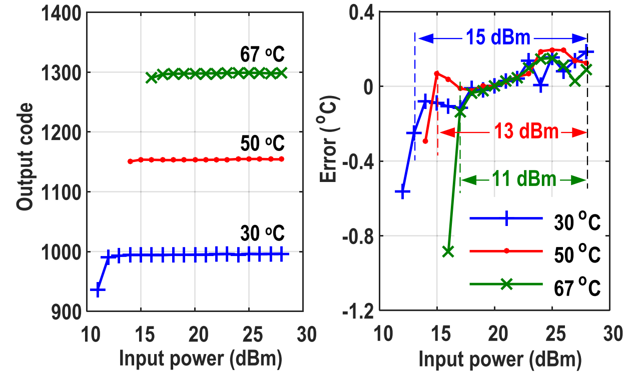


Fig. 16. Sensing error at different incident power levels (wired testing using RFID tester, antenna not matched).

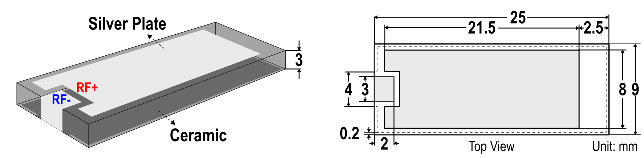


Fig. 17. Designed microstrip patch antenna and its dimensions (not drawn to scale).

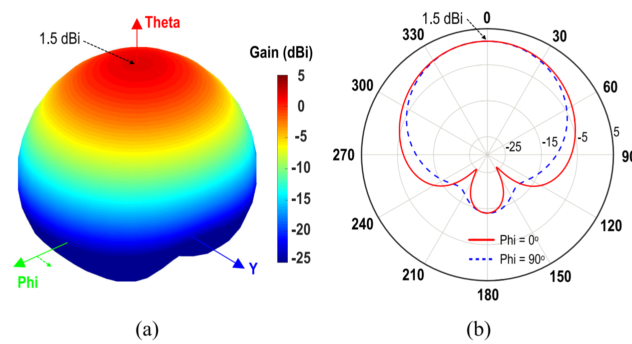


Fig. 18. Simulated 3-D (a) and 2-D (b) radiation pattern (in dBi) of the designed antenna in HFSS.

B. Tag Deployment in the Grid

Grid equipment mostly has conductive metal surface that can cause strong EM antenna-matter interaction [33]. Typical tags cannot receive power and/or transmit information after being deployed in the grid. In this paper, an antimetal side-fed microstrip patch antenna on a ceramic substrate (sintered from a mixture of ZrO_2, MgO, MnO_2, and Sm_2O_3) is designed. Fig. 17 shows the detailed antenna layout and its critical dimensions, in which the length of the silver plate is fine-grained to achieve a conjugate impedance matching with the designed IC. The relative permittivity ε_r of the ceramic is 68 and the thickness of the silver metallic plate is 35 μm (slight variation of the metal thickness does not affect the antenna performance [34]). Fig. 18(a) and (b) is the simulated (in HFSS) three-dimensional (3-D) and

TABLE I
COMPARISON WITH OTHER COMMERCIAL PASSIVE UHF SENSE (TEMPERATURE) ICS AND TAGS

	MagnusS3 [15]	EM4325 [16]	SensTag [17]	Electra-CT [18]	SL900A [19]	This work
Device version	2015	2017	2014	2016	2018	2018
Type	Passive	Passive/BAP	Passive	Passive	Passive/BAP	Passive
†Chip area (mm^2)	<2.56[a]	2.95	n/a	n/a	7.14[f]	1.44
Sensing range	-40 to 85 °C	-40 to 60 °C	-29 to 105 °C	-30 to 85 °C	0 to 40 °C	**-25 to 120 °C**
Inaccurary	±5 °C/±1 °C	±2 °C[c]	±1 °C	±0.5 °C	±1 °C[g]	±2.5 °C (3σ)
Calibration	1-point/2-point	1-point	n/a	n/a	1-point	1-point
‡Relative inaccuracy (%)	8/1.6	4	1.5	0.9[e]	5	3.45
Sensing resolution	0.25 °C[b]	0.25 °C	n/a	>0.1 °C	0.18 °C	0.17 °C
Chip sensing sensitivity	-9.9 dBm	-4.5 dBm	n/a	n/a	-0.7 dBm[h]	**-10.8 dBm**
Tag sensing sensitivity	n/a	n/a	+0.85 dBm[d]	-2 dBm	n/a	**-12.3 dBm**
*Sensing distance	n/a	n/a	1.53 m	2.12 m	n/a	**3.5 m[i]**

†: Fabrication technologies for the commercial products are unknown.
‡: Relative inaccuracy = Inaccuracy/Sensing range × 100%.
*: 4 W EIRP reading power.
a: Estimated from its quad flat no-lead package dimensions and die pad locations.
b: After averaging 139 readings.
c: Calibrated at 5 °C.
d: Estimated with its 5 feet reading distance, a 35% rectifier efficiency and zero path loss.
e: SiP solution, using the 103GT-2 NTC thermistor from Semitec as the sensing device.
f: Includes an external sensor front-end.
g: Measured with no RF field present.
h: Estimated with its 300 μW sensing power and a 35% rectifier efficiency.
i: Filed measurement result when deployed on a metal surface.

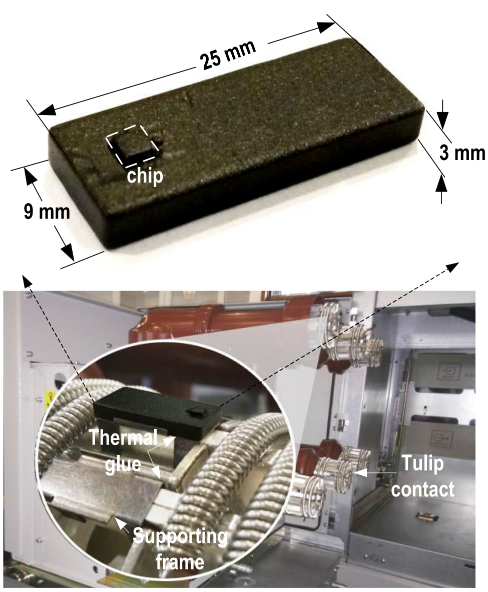


Fig. 19. Antimetal packaged ceramic sense tag and its deployment on a ring main unit.

two-dimensional (2-D) (at Phi = 0° and 90°) antenna radiation pattern at 920 MHz, respectively, where an antenna gain of 1.5 dBi is achieved. The designed chip is flip-chip bonded to this antenna [35]. Fig. 19 shows the packaged sense tag with a feature size of 2.5 × 0.9 × 0.3 cm, which can be installed in grid equipment with bolted connection or thermal adhesives. When tested in the ambient environment, the nominal free space sensing distance of this tag is 5.2 m at room temperature with 4 Watts EIRP from a commercial reader (the reader's sensitivity

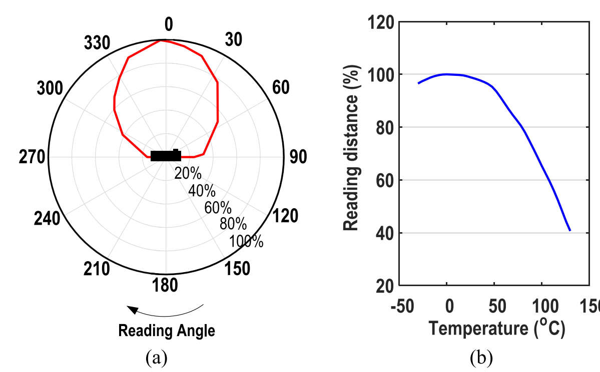


Fig. 20. Measured tag reading distance (normalized) at different reading angles (a) and temperatures (b) when placed on metal surfaces.

is −85 dBm). With the same reading power, the sensing distance of the tag slightly reduces to 3.5 m when deployed on the Tulip contact of a ring main unit in the substation. Fig. 20(a) shows the measured tag reading distance at different reading angles on a metal surface, where 80% reading distance can be maintained for a 60° reading span. At high temperatures, the reading distance also slightly decreases due to the higher tag power consumption [see Fig. 20(b)].

The performance of our tag is summarized in Table I and benchmarked with existing commercial passive UHF sense (temperature) ICs and tags. Note that the comparison between different designs is not that straightforward because the overall system functions, fabrication processes, and optimization targets vary significantly. Meanwhile, some designs (e.g., [17], [18]) use system-in-package (SiP) integration instead of system-on-chip solution, which also affects the overall tag performances. In Table I, as the fabrication processes for commercial products are not disclosed, a direct comparison of chip area for different designs is impossible. However, with the decrease of chip fabrication and package cost, the calibration, deployment, and maintenance cost of a sense tag are of more importance compared to its IC area.

The scope of this paper is to optimize the sensitivity and sensing range of the tag. It can be observed that, compared with [15]–[19], this design features the widest sensing range from −25 to 120 °C with a moderate sensing precision (3.45% relative inaccuracy) after a one-point wireless trim. Meanwhile, because of the overall tag system optimization, the low-power sensor design, and the elimination of power-hungry MTP writing, the proposed tag IC achieves a sensitivity of −10.8 dBm during sensing, which is the state-of-the-art among existing passive tag ICs with embedded temperature sensor[15]–[17], [19]. The packaged tag sensitivity however varies greatly with antenna designs. In this paper, the sensitivity of the packaged tag for grid application is −12.3 dBm using a 1.5 dBi ceramic antenna. The sensing resolution of this tag is in line with [19] and is better than [15] and [16]. In Table I, Farsens [18] showed a superior inaccuracy of 0.9% since it employs an SiP solution with an accurate NTC thermistor as its sensing device. This is an advantage of SiP but at the cost of a bulky package (6.6 × 5 × 1.5 cm) and lower sensitivity. The precision of our design is lower than [17] and could be improved by adopting dynamic error correction and nonlinear compensation techniques in the sensing front-end.

IV. Conclusion

This paper presented a passive UHF sense tag that had a high sensing sensitivity and a moderate sensing precision. Assisted by the precharge scheme and the process compensation of the sensor clock, a small incident-power-dependent sensing error was also achieved. The ceramic packaged tag exhibits robust operation when tested in a high-voltage substation and achieved a sensing distance of 3.5 m. The combination of passive and wireless operation, high sensing sensitivity, wide sensing range, and small incident-power-dependent error makes this tag a safe and low-cost solution for electrical grid and substation thermal monitoring applications with minimal infrastructure renovations.

Acknowledgment

The authors would like to thank Mr. Q. Zhu, Mr. X. Tang, and Mr. S. Lin for performing the chip testing. The publication of this article was funded by the Qatar National Library.

References

[1] G.-M. Ma *et al.*, "A wireless and passive online temperature monitoring system for GIS based on surface-acoustic-wave sensor," *IEEE Trans. Power Del.*, vol. 31, no. 3, pp. 1270–1280, Jun. 2016.

[2] D. A. Genutis, "Top five switchgear failure causes and how to avoid them," Netaworld, 2010. [Online]. Available: http://www.netaworld.org/sites/default/files/public/neta-journals/NWsu10-NoOutage-Genutis.pdf. Accessed on: May 2018.

[3] "Monitor switchgear temperatures to improve safety and reduce costs," Tech. Rep. WP006F10, RFMicron, Austin, TX, USA, Jun. 2017.

[4] S. DeGrate, J. Payne, and R. Belak, "Thermal imaging: Just a note, not the whole tune," *IEEE Ind. Appl. Mag.*, vol. 21, no. 4, pp. 26–35, Apr. 2015.

[5] National Instruments, Fundamentals of fiber Bragg grating (FBG) optical sensing, 2018. [Online]. Available: http://www.ni.com/white-paper/11821/en/. Accessed on: May 2018.

[6] G. M. Ma *et al.*, "Distributed partial discharge detection in a power transformer based on phase-shifted FBG," *IEEE Sensors J.*, vol. 18, no. 7, pp. 2788–2795, Apr. 2018.

[7] Y. W. Shang, H. Y. Li, J. H. Wang, J. D. Wu, and X. N. He, "Analysis and design of a current transformer fed power supply from high AC voltage cable," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 177–182.

[8] V. C. Gungor, B. Lu, and G. P. Hancke, "Opportunities and challenges of wireless sensor networks in smart grid," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3557–3564, Oct. 2010.

[9] J. Yin *et al.*, "A system-on-chip EPC Gen-2 passive UHF RFID tag with embedded temperature sensor," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2404–2420, Nov. 2010.

[10] IEEE Std C37.23-2015, IEEE standard for metal-enclosed bus, Dec. 2015.

[11] IEEE Std C37.13-2015, IEEE standard for low-voltage AC power circuit breakers used in enclosures, Dec. 2015.

[12] NFPA 70E: Standard for electrical safety in the workplace, 2018. [Online]. Available: https://www.nfpa.org/. Accessed on: Jun. 2018.

[13] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[14] Impinj. *Datasheet of monza R6*, 2017. [Online]. Available: https://support.impinj.com/hc/en-us/articles/202765328-Monza-R6-Product-Brief-Datasheet

[15] SmartRAC. *Passive Sensors Technical Guide*, AN-FAM1601 Application Note, Oct. 2016.

[16] EM Microelectronic. *Datasheet of EM4325*, 2017. [Online]. Available: http://www.emmicroelectronic.com/sites/default/files/public/products/datasheets/4325-ds_0.pdf.

[17] Phase IV Inc. *Datasheet of SensTag*, 2014. [Online]. Available: https://www.phaseivengr.com/wp-content/uploads/2014/02/61-100042_-Data-Sheet-UHF-RFID-Surface-Temp-Kit.pdf.

[18] Farsens. *Datasheet of Electra-CT*, 2016. [Online]. Available: http://www.farsens.com/wp-content/uploads/2016/10/DS-ELECTRA-CT-V01.pdf

[19] AMS AG. *Datasheet of SL900A*, 2018. [Online]. Avaibable: https://ams.com/documents/20143/36005/SL900A_DS000294_4-00.pdf

[20] EPCglobal, "Radio-frequency identity protocols generation-2 UHF RFID specification for RFID air interface protocol for communications at 860 MHz-960 MHz Version 2.0.1 Ratified," 2015.

[21] T. Yang *et al.*, "An active tag using carrier recovery circuit for EPC Gen2 passive UHF RFID systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8925–8935, Nov. 2018.

[22] M. Chen *et al.*, "A self-powered 3.26-μW 70-meter wireless temperature sensor node for power grid monitoring," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8956–8965, Nov. 2018.

[23] B. Wang, M. K. Law, A. Bermak, and H. C. Luong, "A passive RFID tag embedded temperature sensor with improved process spreads immunity for a −30 °C to 60 °C sensing range," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 337–346, Feb. 2014.

[24] Synopsys. *MTP ULP NVM*. [Online]. Available: https://www.synopsys.com/dw/ipdir.php?ds=nvm_mtp_rfid

[25] ON Semiconductor, *Battery Free Wireless Sensor Measurements, Application Note*, 2016. [Online]. Available: http://www.onsemi.com/pub/Collateral/AND9211-D.pdf

[26] K. Yang *et al.*, "A 0.6 nJ −0.22/+0.19 °C inaccuracy temperature sensor using exponential subthreshold oscillation dependence," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2017, pp. 160–161.

[27] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.

[28] M. Pertijs and J. Huijsing, *Precision Temperature Sensors in CMOS Technology*, 1st ed. Dordrecht, Netherlands: Springer, 2006, pp. 31–54.

[29] K. Souri, Y. Chae, and K. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ±0.15 °C (3σ) from -55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[30] G. Wang, A. Heidari, K. A. A. Makinwa, and G. C. M. Meijer, "An accurate BJT-based CMOS temperature sensor with duty-cycle-modulated output," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 1572–1580, Feb. 2017.

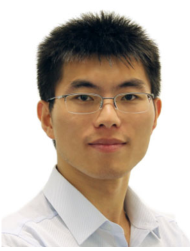
[31] Y. Hsu, C. Tai, M. Chuang, A. Roth, and E. Soenen, "An 18.75 μW dynamic-distributing-bias temperature sensor with 0.87 °C (3σ) untrimmed inaccuracy and 0.00946 mm^2 area," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2017, pp. 102–103.

[32] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002, p. 182.

[33] H. H. Yeh, Y. C. Hung, J. J. Yu, H. C. Lin, and C. H. Chen, "Antimetal RFID tag and manufacturing method thereof," *U.S. Patent* 20090160653A1, Dec. 2007.

[34] T. Bjorninen, L. Sydanheimo, L. Ukkonen, and Y. Rahmat-Samii, "Advances in antenna designs for UHF RFID tags mountable on conductive items," *IEEE Antennas Propag. Mag.*, vol. 56, no. 1, pp. 79–103, Feb. 2014.

[35] J. Choo and J. Ryoo, "Analysis of flip chip bonding for performance stability of UHF RFID tags," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 4, no. 10, pp. 1714–1721, Oct. 2014.



Bo Wang (S'12–M'16) received the B.Eng. degree (Hons.) in electrical engineering from Zhejiang University, Hangzhou, China, in 2010, M.Phil. and Ph.D. degrees in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2012 and 2015, respectively.

In 2015, he joined HKUST as a Postdoctoral Researcher and leaded the HKUST-MIT consortium project on wireless sensing node design for smart green building applications. Afterwards, he was with the Massachusetts Institute of Technology in 2016 on low-power data converter for this project. In 2017, he joined Hamad Bin Khalifa University, Qatar Foundation, as a Founding Faculty, where he is currently an Assistant Professor with the Division of Information and Computing Technology, College of Science and Engineering. His research interests include energy-efficient analog mixed-signal circuits, sensor and sensor interface, and heterogeneous integrated systems for *in vitro/vivo* health monitoring.

Dr. Wang was the recipient of the IEEE ASP-DAC Best Design Award in 2016.

Man-Kay Law (M'11–SM'16) received the B.Sc. degree in computer engineering and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2006 and 2011, respectively.

In 2011, he joined HKUST as a Visiting Assistant Professor. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal Very large scale integration (VLSI), Faculty of Science and Technology, University of Macau, Macao. He developed an ultra-low power fully integrated CMOS temperature sensing passive ultra-high-frequency (UHF) radio-frequency identification tag (RFID) tag together with Zhejiang Advanced Manufacturing Institute and HKUST. He has authored and coauthored more than 80 technical journals and conference papers and holds six U.S. patents. His research interests include the development of ultra-low power sensing circuits and integrated energy harvesting techniques for wireless and biomedical applications.

Prof. Law is a member of the Technical Program Committee of Asia Symposium on Quality Electronic Design, IEEE International Symposium on Circuits and Systems, Biomedical Circuits and Systems Conference, International Symposium on Integrated Circuits, and the University Design Contest Co-Chair of Asia and South Pacific Design Automation Conference. He was a co-recipient of the ASQED Best Paper Award in 2013, A-SSCC Distinguished Design Award in 2015, and ASPDAC Best Design Award in 2013. He also received the Macao Science and Technology Invention Award (2nd Class) by Macau Government - FDCT in 2014 and 2018. He serves as a technical committee member in both the IEEE CAS committee on Sensory Systems as well as Biomedical Circuits and Systems. He is currently an ITPC member of the IEEE International Solid-State Circuits Conference.

Jun Yi (S'03–M'09) received the B.Sc. and M.Sc. degrees in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2001 and 2004, respectively, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology (HKUST), Hong Kong, China, in 2010.

He worked in HKUST as a Research Associate in 2010. In 2010, he joined Texas Instruments Semiconductor Technologies (Shanghai), China, as an Analog Design Engineer working for computing power dc–dc and high-speed interface product lines. From 2014 to 2017, he was with InMicro Micro-electronics (Xiamen) as a Design Department Director. He is currently with Zhejiang Yuehe Technology, focusing on passive and wireless sensor design. His research interests include ultra-low-power analog and mixed-signal integrated circuits and power management systems, with emphasis on wireless microsensor radio-frequency identification tag (RFID), biomedical, and mobile applications.

Chi-Ying Tsui (SM'11) received the B.S. degree in electrical engineering from the University of Hong Kong, Hong Kong, in 1982, and the Ph.D. degree in computer engineering from the University of Southern California, Los Angeles, CA, USA, in 1994.

He joined the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, in 1994, where he is currently a Full Professor. He has authored more than 200 refereed publications and holds ten U.S. patents on power management, VLSI, and multimedia systems. His current research interests include designing very large scale integration architectures for low-power applications and developing energy harvesting and power management circuits and techniques for ultra-low-power embedded systems.

Dr. Tsui received the Best Paper Awards from the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, IEEE International Symposium on Circuits and Systems, IEEE/Association for Computing Machinery International Symposium on Low Power Electronics and Design, and IEEE DELTA and CODES. He also received the Design Awards from the IEEE ASP-DAC University Design Contest in 2004 and 2006, respectively.

Amine Bermak (M'99–SM'04–F'13) received the M.Eng. and Ph.D. degrees in electronic engineering from Paul Sabatier University, Toulouse, France, in 1994 and 1998, respectively.

He was with the LAAS-CNRS, French National Research Center, Microsystems and Microstructures Research Group, where he developed a 3-D Very large scale integration (VLSI) chip for artificial neural network classification and detection applications. He joined the Advanced Computer Architecture Research Group, York University, York, U.K., where he held a Post-Doctoral position on VLSI implementation of CMM neural network for vision applications in a project funded by the British Aerospace. In 1998, he joined Edith Cowan University, Perth, Australia, as a Research Fellow in smart vision sensors, and a Senior Lecturer with the School of Engineering and Mathematics. He served as a Professor with the Electronic and Computer Engineering Department, Hong Kong University of Science and Technology, where he also served as the Director of Computer Engineering and the Director of the M.Sc. degree program in integrated circuit design. He is currently a Professor with the College of Science and Engineering, Hamad Bin Khalifa University, Doha, Qatar. His research interests include VLSI circuits and systems for signal, image processing, sensors, and microsystems application.

Dr. Bermak is currently serving on the Editorial Board of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and IEEE TRANSACTIONS ON ELECTRON DEVICES. He is also an Editor of *Scientific Reports (Nature)*. He is an IEEE Distinguished Lecturer.